REMARKS/ARGUMENTS

The above-identified patent application has been reviewed in light of the Examiner's Action dated August 25, 2006. Claims 1, 5, 7, 8, 10 and 18 have been amended. Claims 2 - 4, 6, 9, 12 - 17 are canceled, without intending to abandon or to dedicate to the public any patentable subject matter. Claims 19 - 30 are new. Accordingly, Claims 1, 5, 7, 8, 10, 11 and 18 - 30 are now pending. As set forth herein, reconsideration and withdrawal of the objections to and rejections of the claims are respectfully requested.

The Examiner has objected to the drawings for failing to show every feature of the invention specified in the claims. In that regard, the attached sheet of drawings includes changes to Fig 1.In the amended Fig. 1, two stacking faults, each of which is denoted by a reference sign lX, are added. Together with the amendment of Fig. 1, the specification is amended to change "stacking faults" on page 19, line 8 to "stacking faults, each of which is denoted by a reference sign 1X."

These amendments are supported by the specification and do not constitute new matter. In particular, these amendment are based on the paragraph starting on page 18, line 16 and ending on page 19, line 24 in the English translation that corresponds to paragraph 0027 of PCT/JP2004/011936. Moreover, as is well known to those skilled in the art, stacking faults are formed in parallel with the basal plane *i.e.* (0001) crystal face according to their property. For example, the (0001) crystal, not shown in Fig. 1, is inclined 3 to 8 degrees with respect to face n-type semiconductor region 2 and p-type semiconductor region 3. Therefore, stacking faults 1X are also inclined 3 to 8 degrees with respect to n-type semiconductor region 2 and p-type semiconductor region 3. Please note that, in Fig. 1, the scale in a longitudinal direction is enlarged in comparison to the scale in a transverse direction.

The Examiner has objected to Claims 1, 7 and 18 for containing informalities. Additionally, the Examiner has objected to Claims 5, 7 and 8 for failing to provide antecedent basis for the claimed subject matter. In that regard, throughout the claims "heating means for heating" is changed to "means for heating."

The Examiner has stated that the limitation "means for heating" is construed to cover the elements disclosed in the specification at pg. 27, ln. 7-11 and pg. 51, ln. 13-15. It is noted that the "means for heating" is not limited to those elements cited by the Examiner. In particular, the specification discloses several examples of heaters or means for heating including heater 15 (beginning at pg. 27, ln. 7), heater 46 (beginning at pg. 36, ln. 1), heater 85 (beginning at pg. 44, ln. 5) and heater 127 (beginning at pg. 59, ln. 18). Additionally, other examples of means for heating are given on pg. 62, ln. 12 through pg. 63, pg. 9.

Claim 1, 8, 11 and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over JP-2002-325355 to Sugawara ("Sugawara '55") in view of "Recent Progress in Sic Power Device Developments and Application studies," April 14- 17.2003, Cambridge, UK, pp. 10- 18 by Sugawara et al. ("Sugawara '03"). Claims 1, 5, 7, 10, 11 and 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Sugawara '55 in view of JP 9-148681 to Tato ("Tato"). In order to establish a *prima facie* case of obviousness under § 103, there must be some suggestion or motivation to modify the reference or to combine the reference teachings, there must a reasonable expectation of success, and the prior art reference or references must teach or suggest all the claim limitations. (MPEP § 2143.) However, all of the elements of the claims as amended cannot be found in the cited references, whether those references are considered alone or in combination. Accordingly, reconsideration and withdrawal of the rejections of the claims as obvious in view of the cited references are respectfully requested.

In independent Claims 1 and 18, "a wide-gap semiconductor" is amended to recite "a wide-gap semiconductor having stacking faults resulting from basal lane dislocation." This amendment is based on a paragraph from page 18, line 16 to page 19, line 24 in English translation that corresponds to a paragraph 0027 of PCT/JP2004/011936. In addition, "125°C" in Claim 1 is changed into "50°C", as well as in Claims 5, 8, 10 and 18. This amendment is based on a paragraph from page 19, line 25 to page 20, line 14 in English translation that corresponds to a paragraph 0028 of PCT/ JP2004/0 1 1936.

The Examiner states that in view of the teachings of Sugawara '03, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Sugawara '55 by

incorporating a heat sink, so as to reduce the built-in potential and lower total power loss of as taught by Sugawara '03 (page 15, left col., first par.). Moreover, in rejecting Claim 17, the examiner states that "Sugawara '03 discloses (page 12, numeral 111) that several Sic crystal defects" and "stacking faults are one type crystal defects." However, the crystal defects discussed in Sugawara '03 differ in important respects from the stacking faults associated with the claimed invention. In particular, in the amended claims, the wide-gap semiconductor and accordingly the wide-gap bipolar semiconductor element have stacking faults resulting from basal plane dislocation.

It is true that stacking faults are one type of crystal defect as the examiner states. However, other crystal defects not resulting from basal plane dislocation, for example, micropipes, spiral dislocations, threaded dislocations, carrot defects and the like do not have the property that their regions spread out as a current passes over them. On the contrary, as is shown in Figs. A1 to A2 below, stacking faults resulting from basal plane dislocation have the property that their regions spread out in a fan-like or triangular shape in a plane parallel to the basal plane

Fig. A1

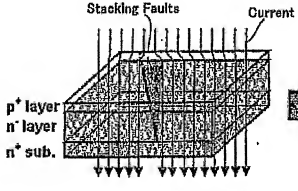


Fig. A2

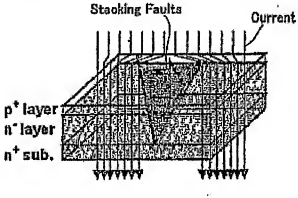


Fig. B1

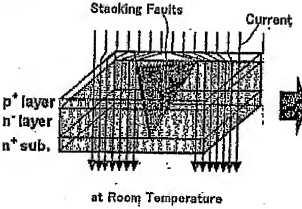
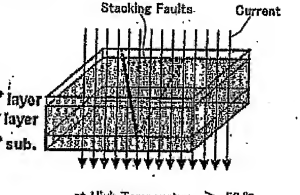


Fig. B2



as current passes over them. As is shown in Figure B1, each of the stacking faults that has spread out becomes an obstacle on the current path, resulting in an increase of the ON voltage.

For additional information regarding basal plane dislocation and stacking faults the Examiner is referred to "Propagation of Current-Induced Stacking Faults and Forward Voltage Degradation in 4H-Sic PiN Diodes", Materials Science Forum Vol. 389-393 (2002) pp. 427-430 by R.E. Stahlbush et al. The Stahlbush document is submitted concurrently with this paper in an information disclosure statement.

The claimed invention is based on the technical idea that adverse effects due to the stacking faults resulting from basal plane dislocation can be prevented by heating said semiconductor element at a temperature of 50°C or more. Adverse effects prevented by the claimed invention include an increase of the ON voltage and destruction of the semiconductor element. As is shown in Figure B2 above, at the temperature of 50°C or more, the stacking faults resulting from basal plane dislocation performs as if they were not present, resulting in no increase of the ON voltage.

In Sugawara '03, there is only a description that "The Sic pn diode has a higher built-in potential, but it can be reduced by increasing the device temperature with a very compact heat sink," (See page 15, left col., first par.). This description just discloses an idea to reduce the ON voltage by decreasing the built-in potential utilizing the temperature characteristics of the wide-gap semiconductor, and does not disclose any idea to reduce the ON voltage by resolving the adverse effects due to the stacking faults resulting from basal plane dislocation. As described above, the defects such as micropipes in Sugawara '03 do not have the property that their regions spread out as a current passes over them. Therefore, based on the combination of Sugawara '55 and Sugawara '03 one of ordinary skill in the art would not come up with the idea to prevent the increase of the ON voltage and destruction of the semiconductor element having stacking faults resulting from basal plane dislocation by heating the semiconductor element.

Therefore, even if Sugawara '03 is combined with Sugawara '55, the claimed invention is not taught, suggested or described. Moreover, Tato also does not disclose the stacking faults resulting from basal plane dislocation, and therefore, does not disclose reducing the ON voltage by resolving the adverse effects due to the stacking faults resulting from basal plane dislocation. Therefore, even

if Tato is combined with Sugawara 55, the claimed invention is not taught, suggested or described. Accordingly, reconsideration and withdrawal of all rejections under 35 U.S.C. §103(a) are respectfully requested.

Moreover, with regards to Claims 5, 7, 8, 10, 11, 19 - 22 and 26 - 30, these claims are directly or indirectly dependent on amended Claim 1. Therefore, Claims 5, 7, 8, 10, 11, 19-22, and 26-30 should not be rejected under 35 U.S.C. §103(a). With regards to Claim 18, this claim substantially comprises all of the subject matter of Claim 1, although Claim 18 is an independent claim. Therefore, Claim 18 should not be rejected under 35 U.S.C. §103(a).

New Claims 19-30 are added. Claims 19-22 are directed to a semiconductor device comprising a specified semiconductor package. Claims 23 - 25 are directed to an operation method for a semiconductor device or a wide-gap bipolar semiconductor element. Claims 26-30 are directed to a semiconductor device wherein the "means for heating" is defined concretely. In particular, Claim 19 comprises a support made of metal. This amendment is based on Fig. 1 and a paragraph from page 26, line 15 to page 27, line 6 in English translation that corresponds to a paragraph 0037 of PCT/JP2004/011936. An advantage of Claim 19 is that the temperature of the semiconductor element can be raised rapidly.

Claim 20 comprises a cap made of metal fixed on the support. This amendment is also based on Fig. 1 and a paragraph from page 26, line 15 to page 27, line 6 in English translation that corresponds to a paragraph 0037 of PCT/JP2004/0 11936. An advantage of Claim 20 is that the temperature of the element can be raised rapidly and uniformly.

Claim 21 defines another structure, which also brings an advantage that the temperature of the semiconductor element can be raised rapidly. This amendment is based on paragraphs from page 26, line 15 to page 27, line 15 in English translation that correspond to paragraphs 0037 and 0038 of PCT/JP2004/011936.

Claim 22 defines another structure. This amendment is based on Fig. 7 and a paragraph from page 58, line 19 to page 59, line 4 in English translation that corresponds to a paragraph 0090 of PCT/ JP2004/0 1 1936. An advantage of Claim 22 is that insulation between semiconductor element and the support is ensured.

Claim 23 comprises three steps of: i) heating the semiconductor element at a first temperature of 50°C or more and less than 200°C before energization, ii) after a start of the energization, operating the semiconductor element with an applied current smaller than a rated current until the semiconductor element reaches a second temperature of 200°C or more, iii) then allowing the semiconductor element to be applied with a current up to the rated current. This amendment is based on a paragraph from page 20, line 15 to page 21, line 2 and a paragraph from page 56, lines 10-18 in the English translation that correspond to paragraphs 0029 and 0083 of PCT/JP2004/011936, respectively. An advantage of Claim 23 is that, even in the case that the wide-gap bipolar semiconductor element has stacking faults resulting from basal plane dislocation, the rising of the ON voltage owing to the stacking faults and the significant increase of the steady loss caused thereby can be avoided.

Claim 24 depends from Claim 23 and is characterized in that, at-the above step ii), the temperature of the semiconductor element is raised by the means for heating in addition to self-heating of the semiconductor element. This amendment is based on a paragraph from page 21, line 3 to page 22, line 3 in the English translation that corresponds to a paragraph 0030 of PCT/ JP2004/011936. An advantage of Claim 24 is to increase the above advantage of Claim 23.

Claim 25 comprises two steps of: i) operating the wide-gap- bipolar semiconductor element with an applied current smaller than a rated current until the semiconductor element reaches a temperature of 200°C or more; ii) then allowing the element to be applied with a current up to the rated current. This amendment is based on a paragraph from page 21, line 3 to page 22, line 3 and a paragraph from page 56, lines 10- 18 in the English translation that correspond to paragraphs 0030 and 0083 of PCT/ JP2004/011936, respectively.

With regards to Claims 23, 24 and 25, these claims are directed to an operation method for a semiconductor device. Claim 23 cites a semiconductor device according to Claim 1, and Claim 24 depends on it. They show the same advantages as those of Claim 1. Therefore, Claims 23 and 24 should not be rejected under 35 U.S.C. §103(a).

Claim 25 is an independent claim. Herein, Claim 25 is directed to an operation method for a wide-gap bipolar semiconductor element using a wide-gap semiconductor having stacking

faults resulting from basal plane dislocation, as is in the case of Claim 1. And therefore, Claim 25 shows the same advantages as those of Claim1. Namely, reducing the ON voltage by resolving the adverse effects due to the stacking faults resulting from basal plane dislocation by heating the semiconductor element. Therefore, Claim 25 should not be rejected under 35 U.S.C. §103 (a).

In Claim 26, said means for heating is a radiant heating section. In Claim 27, said means for heating comprises blowing hot air to the semiconductor package. In Claim 28 and 29, said means for heating is an induction heating apparatus. The reason why Claim 28 depends on Claim19 and Claim 29 depends on Claim 20, respectively, is induction heating requires that the semiconductor package i.e. the support or the cap be made of metal. These amendments are based on a paragraph from page 62, line 12 to page 63, line 9 in English translation that correspond to paragraphs 0098 of PCT/ JP2004/011936.

In Claim 30, the semiconductor package comprises a molded heat resistant resin. This amendment is based on a paragraph from page 63, line 10 to page 64, line 6 in English translation that correspond to a paragraph 0099 of PCT/JP2004/011936.

The application now appearing to be in form for allowance, early notification of the same is respectfully requested. The Examiner is invited to contact the undersigned by telephone if doing so would be of assistance.

Respectfully submitted,

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